ABSTRACT

A processor for processing an interruptible repeat instruction is provided. The repeat instruction may include an immediate operand specifying a loop count value corresponding to the number of times that the loop is to be repeated. Alternatively, the repeat instruction may include an address of a register which holds the loop count value. The instruction immediately following the repeat instruction is the target instruction for repetition. The processing includes repeating execution of the target instruction according to the loop count value in a low processor cycle overhead manner. The processing may also include handling interrupts during repeat instruction processing in a low-overhead manner during the initial call of the interrupt service routine as well as upon returning from the interrupt service routine.